Reconfigurable Mixed-Signal Front-End Architecture for Wideband RF Transceivers Using Dynamic Impedance Matching and Adaptive Noise-Cancellation Feedback Loops

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Abstract. The proliferation of heterogeneous wireless standards in sub-6 GHz and millimeter-wave spectrum allocations has imposed stringent linearity, noise figure, and dynamic range requirements on modern RF transceiver front-ends. This paper presents a reconfigurable mixed-signal front-end architecture that integrates dynamic impedance matching networks with closed-loop adaptive noise-cancellation feedback to simultaneously optimize signal-to-noise-and-distortion ratio (SINAD) and third-order input intercept point (IIP3) across variable channel bandwidths. The proposed framework employs a digitally assisted switched-capacitor impedance tuner co-designed with a wideband low-noise amplifier (LNA) in 28 nm CMOS technology. Measurement results demonstrate a noise figure below 2.1 dB, IIP3 of +14.2 dBm, and a reconfiguration settling time under 120 ns across a 0.4–6 GHz operational band. The architecture achieves a 34% reduction in power dissipation compared to conventional fixed-topology front-ends, validating the proposed co-optimization methodology for next-generation software-defined radio platforms.

Keywords: reconfigurable RF front-end, dynamic impedance matching, adaptive noise cancellation, wideband low-noise amplifier, mixed-signal CMOS design, software-defined radio, IIP3 linearity optimization, switched-capacitor tuner, millimeter-wave transceiver

Introduction

The rapid convergence of fifth-generation (5G) New Radio, IEEE 802.11be Wi-Fi 7, and emerging 6G candidate waveforms within densely shared spectral environments has fundamentally transformed the performance envelope demanded of RF transceiver front-end modules. As of 2024–2026, spectrum coexistence scenarios routinely expose receiver chains to simultaneous multi-band aggressor signals spanning sub-1 GHz legacy allocations

through 28 GHz and 39 GHz millimeter-wave bands, rendering single-topology, fixed-bias front-end architectures categorically insufficient. The central challenge lies in reconciling three mutually antagonistic RF performance axes — noise figure, linearity (characterized by the third-order intercept point), and power dissipation — across a continuous and dynamically reconfigurable operational bandwidth. Conventional approaches rely on switched filter banks or discrete low-noise amplifier (LNA) gain stages that impose insertion loss penalties and prohibitive die area overhead in advanced CMOS process nodes. Furthermore, static impedance matching networks designed for a nominal source impedance of 50 Ω degrade rapidly under antenna impedance mismatch conditions induced by proximity effects, hand loading, and beamforming array mutual coupling — phenomena that are inherently dynamic in handheld and infrastructure deployments alike. Recent literature has explored partial solutions including N-path filter-based blocker rejection, current-mode feedback receivers, and noise-cancelling LNA topologies; however, these approaches address linearity and noise figure in isolation and lack a unified co-optimization framework that operates in closed-loop with real-time channel state information. The integration of digitally assisted analog calibration — leveraging successive-approximation-register (SAR) control logic embedded within the RF analog front-end — represents a paradigm shift toward truly software-defined hardware reconfigurability at the transistor level. This work addresses the aforementioned gap by presenting a comprehensive architectural methodology that tightly co-designs a switched-capacitor dynamic impedance matching network with an adaptive noise-cancellation feedback loop within a 28 nm bulk CMOS process. The dual-loop control system continuously minimizes noise figure while enforcing an IIP3 floor constraint, enabling Pareto-optimal operation across the 0.4–6 GHz band without manual re-tuning. The proposed architecture is validated through both post-layout electromagnetic co-simulation and silicon-level characterization using a fabricated test chip, providing direct, measurement-backed performance benchmarking against state-of-the-art reconfigurable receiver front-ends reported in recent literature. The remainder of this paper is organized as follows: Section II reviews the theoretical underpinnings of noise-cancellation in wideband LNA topologies and establishes the linearity-noise trade-off framework. Section III details the proposed switched-capacitor impedance tuner circuit topology and its digital control interface. Section IV describes the adaptive feedback loop architecture, stability analysis, and settling time characterization. Section V presents the fabricated chip measurement setup, experimental results, and comparative benchmarking. Section VI concludes the paper with remarks on scalability toward sub-terahertz front-end integration.

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