Mitigating Substrate Coupling-Induced Phase Noise Degradation in Millimeter-Wave VCOs Fabricated on Bulk CMOS 28 nm Technology

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Abstract. Phase noise degradation caused by substrate coupling remains a critical bottleneck in the design of millimeter-wave voltage-controlled oscillators (VCOs) implemented on bulk CMOS 28 nm process nodes. This paper presents a systematic methodology for characterizing and suppressing substrate-borne interference pathways using differential guard-ring architectures combined with triple-well isolation structures. An analytical model correlating substrate resistivity gradients with oscillator phase noise spectral density is derived and validated against post-layout electromagnetic simulations performed in Cadence Virtuoso and HFSS. Fabricated prototypes operating in the 57–64 GHz band demonstrate a phase noise of −118 dBc/Hz at 1 MHz offset, representing a 9.4 dB improvement over conventional topologies. The proposed isolation strategy achieves a figure-of-merit of −189 dBc/Hz while consuming 14.2 mW from a 0.9 V supply, confirming the practical viability of the approach for 5G mmWave front-end integration.

Keywords: millimeter-wave VCO, substrate coupling, phase noise, bulk CMOS 28 nm, triple-well isolation, guard-ring architecture, 5G front-end integration, electromagnetic interference suppression, mmWave oscillator design

Introduction

The rapid proliferation of fifth-generation (5G) and emerging sixth-generation (6G) wireless communication infrastructures has placed unprecedented demands on millimeter-wave (mmWave) integrated circuit design, particularly within the 57–71 GHz unlicensed band designated for high-throughput short-range links. Voltage-controlled oscillators (VCOs) constitute a cornerstone of phase-locked loop (PLL) architectures embedded in mmWave transceiver front-ends, and their phase noise performance directly governs system-level error vector magnitude (EVM), adjacent channel leakage ratio (ACRL), and ultimately the achievable spectral efficiency of high-order modulation schemes such as 256-QAM and 1024-QAM. As semiconductor foundries continue to scale CMOS process nodes toward 28 nm and below to leverage increased transit frequency (fT) and maximum oscillation frequency (fmax), a fundamentally adverse consequence emerges: the substrate resistivity of standard bulk CMOS wafers, typically in the range of 10–20 Ω·cm, creates low-impedance parasitic conduction paths that couple switching noise from digital logic blocks, power management units, and neighboring RF circuits directly into the sensitive LC tank of the oscillator. This substrate-mediated interference manifests as a pronounced elevation of the close-in phase noise floor, degrading the $1/f^3$ corner frequency and severely impairing the oscillator's figure-of-merit (FoM). Despite substantial prior art addressing passive isolation techniques — including deep n-well guard rings, patterned ground shields (PGS), and proton-implanted high-resistivity substrates — the quantitative relationship between spatially non-uniform substrate resistivity gradients induced by process variations and the resultant phase noise spectral density has not been rigorously modeled in the context of 28 nm bulk CMOS. Existing empirical correction factors embedded in commercial process design kits (PDKs) inadequately capture the frequency-dependent skin-effect modulation of substrate impedance at frequencies exceeding 50 GHz, leaving designers reliant on iterative post-fabrication tuning. Furthermore, the co-integration of analog RF blocks with dense digital baseband logic on the same die — a trend accelerated by the cost pressures of consumer mmWave chipsets — amplifies substrate injection currents by orders of magnitude compared to standalone RF test structures. This work addresses these challenges through a three-pronged strategy: (i) derivation of a closed-form analytical model for substrate coupling transfer impedance as a function of guard-ring geometry, well doping profile, and operating frequency; (ii) co-simulation of the full electromagnetic substrate model with the nonlinear VCO circuit to predict phase noise degradation at the system level; and (iii) experimental validation through tape-out and characterization of fabricated prototypes in TSMC 28 nm bulk CMOS technology. The remainder of this paper is organized as follows: Section 2 reviews the theoretical background of substrate noise coupling mechanisms and prior isolation methodologies. Section 3 presents the proposed analytical model and its derivation. Section 4 describes the VCO circuit topology and layout implementation of the triple-well isolation scheme. Section 5 details the simulation framework and post-layout verification results. Section 6 reports measured experimental data from fabricated prototypes and benchmarks the

achieved phase noise against the state of the art. Section 7 concludes with design guidelines applicable to mmWave SoC integration.

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