Gate Dielectric Stack Benchmarking in Sub-3 nm FinFET vs. Gate-All-Around Nanosheet FETs: Trade-offs in Interface Trap Density, EOT Scaling, and NBTI Degradation Kinetics

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Abstract. As CMOS technology nodes push below 3 nm, the selection of high-κ gate dielectric architectures in FinFET and gate-all-around (GAA) nanosheet field-effect transistors (NSFETs) presents critical trade-offs between equivalent oxide thickness (EOT) scaling, interface trap density (Dit), and negative bias temperature instability (NBTI) reliability. This study systematically benchmarks HfO_2-based and $HfZrO_x$-based dielectric stacks integrated with TiN metal gates across both device topologies under accelerated aging conditions at 125 °C. Employing charge pumping spectroscopy, time-dependent dielectric breakdown (TDDB) analysis, and capacitance–voltage profiling, we demonstrate that GAA NSFETs exhibit a 23% lower Dit at the Si/SiO_2 interfacial layer compared to FinFET counterparts, while FinFETs retain superior NBTI recovery characteristics at equivalent EOT. These findings provide quantitative design guidelines for process engineers targeting sub-3 nm logic nodes.

Keywords: gate-all-around nanosheet FET, FinFET, high-κ dielectric scaling, equivalent oxide thickness, interface trap density, negative bias temperature instability, TDDB reliability, HfZrOx gate stack, sub-3 nm CMOS technology

Introduction

The relentless downscaling of complementary metal-oxide-semiconductor (CMOS) transistors, governed by Moore's Law trajectories and augmented by the International Roadmap for Devices and Systems (IRDS 2024–2026 edition), has rendered the sub-3 nm logic node one of the most technically demanding frontiers in semiconductor engineering. At these dimensional extremes, conventional planar and even FinFET architectures encounter fundamental electrostatic limitations—most critically, inadequate gate

electrostatic control over the channel, manifesting as drain-induced barrier lowering (DIBL), subthreshold slope degradation, and exponentially rising gate leakage currents. Gate-all-around (GAA) nanosheet field-effect transistors have emerged as the industry-consensus successor architecture, offering a four-sided gate wrap-around topology that maximizes electrostatic integrity per unit footprint. Intel's 20A/18A process node, Samsung's SF3 platform, and TSMC's N2 technology generation have each committed to GAA-based implementations, underscoring the urgency of rigorous comparative characterization between FinFET and GAA paradigms. Central to both architectures is the gate dielectric stack—a multilayer ensemble typically comprising an interfacial SiO_2 or SiON passivation layer, a high-permittivity (high-κ) bulk dielectric such as HfO_2 or compositionally tuned $HfZrO_x$, and a work-function-engineered TiN or TiAlC metal gate electrode. The electrical performance and long-term reliability of this stack are governed by a constellation of interdependent parameters: equivalent oxide thickness (EOT), which directly dictates gate capacitance and drive current; interface trap density (Dit), which modulates threshold voltage variability and subthreshold characteristics; and time-dependent degradation mechanisms, foremost among them negative bias temperature instability (NBTI) and time-dependent dielectric breakdown (TDDB). Prior literature has addressed these phenomena in isolation for legacy nodes, yet a systematic, side-by-side benchmarking under identical process and characterization conditions across FinFET and GAA NSFET topologies at the sub-3 nm regime remains conspicuously absent from the peer-reviewed corpus. This absence is consequential: process integration engineers and device physicists require quantitative, topology-resolved reliability metrics to inform gate stack material selection, thermal budget allocation during dielectric deposition via atomic layer deposition (ALD), and post-deposition anneal (PDA) optimization. The divergence in gate geometry between the fin-based and sheet-based architectures introduces non-trivial differences in thermal conduction, stress-induced defect nucleation at the Si/SiO_2 interface, and trap energy distribution within the high-κ bulk—all of which modulate NBTI kinetics and TDDB lifetime projections in ways that aggregate device models fail to capture. The present work addresses this gap through a rigorous experimental benchmarking campaign. Section II describes the device fabrication splits and dielectric deposition protocols. Section III details the charge pumping spectroscopy, capacitance–voltage (C–V), and accelerated TDDB measurement methodologies. Section IV presents comparative Dit extraction results, NBTI threshold voltage shift (ΔVth) transients, and Weibull statistical lifetime distributions for both topologies. Section V synthesizes these findings into actionable design guidelines, and Section VI concludes with implications for IRDS-aligned technology scaling beyond the 2 nm node.

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