Mitigating Substrate Coupling-Induced Phase Noise Degradation in Millimeter-Wave LC-VCOs Through Deep N-Well Guard Ring Topology Optimization

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Abstract. Substrate coupling remains one of the most persistent sources of phase noise degradation in millimeter-wave LC voltage-controlled oscillators (LC-VCOs) fabricated in bulk CMOS technologies. This paper presents a systematic methodology for characterizing and suppressing substrate-borne interference using optimized deep N-well guard ring geometries integrated within a 28 nm bulk CMOS process node. Electromagnetic co-simulation combining finite-element substrate modeling with Spectre RF periodic steady-state (PSS) noise analysis was employed to quantify coupling attenuation as a function of guard ring segmentation density and well contact pitch. The proposed topology achieves a phase noise reduction of 9.4 dBc/Hz at a 1 MHz offset from a 60 GHz carrier, with a figure-of-merit (FoM) improvement of 6.1 dB over conventional single-ring guard structures, while maintaining a tuning range of 11.3% and a DC power consumption of 18.7 mW.

Keywords: LC voltage-controlled oscillator, substrate coupling suppression, millimeter-wave CMOS, phase noise, deep N-well guard ring, 60 GHz oscillator, figure-of-merit optimization, bulk CMOS substrate modeling, periodic steady-state noise analysis

Introduction

The exponential proliferation of millimeter-wave (mmW) wireless systems—spanning fifth-generation (5G) New Radio deployments at 28 GHz and 60 GHz, IEEE 802.11ad/ay short-range gigabit links, automotive radar at 77 GHz, and emerging 6G candidate bands above 100 GHz—has placed increasingly stringent demands on the spectral purity of on-chip frequency synthesis circuits. Among these, the LC voltage-controlled oscillator represents the most phase-noise-sensitive building block within integer-N and fractional-N phase-locked loops (PLLs), where even marginal degradations in close-in phase noise translate directly into elevated error vector magnitude (EVM) at the system level and, ultimately, into reduced link-budget margins in dense spatial multiplexing environments. In bulk CMOS technology nodes ranging from 65 nm down to 22 nm FD-SOI, the lightly doped p-type substrate acts as a distributed resistive-capacitive network through which digital switching transients, power amplifier drain current harmonics, and supply bounce events couple efficiently into the sensitive LC tank of the oscillator. This phenomenon—commonly termed substrate noise injection—modulates the effective varactor capacitance through the body effect and perturbs the tail-current source operating point, both of which translate into instantaneous frequency deviations that the Leeson model predicts will appear as elevated single-sideband phase noise skirts. Although guard rings fabricated in standard N-well implants provide a partial shielding mechanism by establishing a low-impedance return path for minority carriers, their efficacy degrades sharply above 20 GHz due to the finite quality factor of the well resistance-capacitance ladder and the onset of skin-depth-limited current crowding in the substrate bulk. Prior art addressing this challenge falls broadly into three categories: (i) differential LC tank topologies that exploit common-mode rejection to suppress in-phase substrate perturbations; (ii) post-layout substrate network extraction combined with iterative floor-planning to maximize the physical separation between aggressor and victim circuits; and (iii) active substrate noise cancellation loops that inject a correlated antiphase replica of the interference signal. Each approach entails significant trade-offs in silicon area, design complexity, or power overhead that are incompatible with the area-cost constraints of advanced system-on-chip (SoC) integration at mmW frequencies. The present work addresses this gap by proposing a deep N-well guard ring topology whose segmentation geometry and well contact pitch are co-optimized with respect to substrate coupling transfer impedance across the 10 MHz–10 GHz interference spectrum. The remainder of this paper is organized as follows. Section II develops the distributed substrate network model and validates it against vector network analyzer measurements on dedicated test structures. Section III describes the proposed guard ring topology and the electromagnetic co-simulation methodology. Section IV presents post-layout simulation results for the 60 GHz LC-VCO prototype, benchmarked against state-of-the-art implementations. Section V discusses design scalability toward sub-terahertz applications, and Section VI concludes the paper with key findings and future research directions.

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