

Advanced Techniques in VLSI Design for Low Power Consumption

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Abstract. This article explores advanced techniques in Very Large Scale Integration (VLSI) design aimed at reducing power consumption. The focus is on novel methods that optimize energy efficiency without compromising performance. Through simulations and experimental results, the study demonstrates significant energy savings in integrated circuits. These advancements are crucial for the development of sustainable electronic systems, especially in portable and wireless devices.

Keywords: VLSI Design, Low Power, Energy Efficiency, Integrated Circuits, Dynamic Voltage Scaling

Introduction

The demand for energy-efficient electronic systems has led to a surge in research focused on reducing power consumption in VLSI design. This article delves into innovative approaches to enhance energy efficiency without affecting the performance of integrated circuits. Techniques such as clock gating, power gating, and dynamic voltage scaling are examined in detail. The findings are supported by simulations and empirical data, highlighting potential energy savings. The implications of these techniques extend to portable and wireless devices, where power efficiency is paramount.

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