

Resolving Cache Coherence Violations in Heterogeneous Many-Core Architectures Under Non-Uniform Memory Access Constraints

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Abstract. Cache coherence violations in heterogeneous many-core processors operating under Non-Uniform Memory Access (NUMA) constraints represent a critical bottleneck in high-performance computing systems. This paper presents a formal protocol, designated HeteroSync-CC, for detecting and resolving coherence violations across asymmetric cache hierarchies that couple CPU clusters with integrated GPU tiles. We employ a hybrid directory-based invalidation scheme augmented by a lightweight transactional rollback mechanism to suppress false sharing and stale-read anomalies. Experimental evaluation on a 128-core NUMA testbed demonstrates a 34.7% reduction in coherence traffic overhead and a 21.3% improvement in memory-access latency relative to state-of-the-art MESIF-extended protocols. The proposed protocol is formally verified using TLA⁺ model checking, confirming deadlock-freedom and sequential consistency guarantees under adversarial workload injection.

Keywords: cache coherence protocol, NUMA architecture, heterogeneous many-core systems, directory-based invalidation, transactional memory rollback, false sharing mitigation, TLA⁺ model checking, GPU-CPU memory hierarchy, sequential consistency verification

Introduction

The exponential scaling of transistor density predicted by Moore's Law has given way to an era of architectural heterogeneity, wherein modern computing platforms increasingly integrate diverse processing elements—general-purpose CPU clusters, GPU tiles, neural processing units, and domain-specific accelerators—onto a single die or multi-chiplet substrate. This paradigm shift, while delivering unprecedented raw throughput, introduces profound challenges in maintaining memory consistency across shared cache hierarchies that were originally designed for homogeneous, symmetric multiprocessor systems. In the context of 2024–2026 high-performance computing and data-center deployments, cache coherence violations have emerged as one of the foremost contributors to silent data corruption, non-deterministic execution behavior, and catastrophic performance degradation in production workloads ranging from large-scale machine learning inference to real-time transaction processing. The Non-Uniform Memory Access (NUMA) model, which governs the latency topology of memory regions relative to processing nodes, exacerbates these coherence challenges. When heterogeneous execution units with differing cache line widths, write-combining policies, and prefetch aggressiveness share a physically distributed last-level cache (LLC), classical coherence protocols such as MESI, MOESI, and MESIF encounter state-machine transitions that are either undefined or misspecified for cross-domain interactions. The resulting stale-read anomalies and false-sharing cascades can propagate silently across thousands of execution threads, rendering conventional debugging instrumentation insufficient for root-cause attribution. Prior work has addressed subsets of this problem domain: directory-based coherence schemes have been extended for NUMA topologies, and transactional memory frameworks have offered partial rollback semantics for CPU-centric architectures. However, no unified protocol has simultaneously addressed cross-ISA coherence, asymmetric cache granularity reconciliation, and formal correctness guarantees within a single operational framework applicable to production heterogeneous silicon. This paper closes that gap by introducing HeteroSync-CC, a formally specified cache coherence protocol engineered for heterogeneous many-core platforms operating under NUMA constraints. The protocol couples a hierarchical directory-based invalidation plane with a lightweight, hardware-assisted transactional rollback engine, enabling conflict detection and resolution without stalling the global memory fabric. The remainder of this paper is organized as follows: Section 2 surveys related coherence protocols and identifies their limitations in heterogeneous NUMA contexts; Section 3 presents the HeteroSync-CC protocol specification and its state-machine formalism; Section 4 details the hardware implementation model and microarchitectural integration strategy; Section 5 describes the experimental methodology, testbed configuration, and performance benchmarks; Section 6 reports formal verification results obtained via TLA⁺ model checking; and Section 7 concludes with a discussion of applicability, limitations, and directions for future research.

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